REMARKS

This paper is being provided in response to the Office Action mailed February 9, 2005, for the above-referenced application. In this response, Applicant has cancelled claims 2 and 8 (claims 12-19 having been previously cancelled) without prejudice or disclaimer of the subject matter thereof and amended claims 3, 4, 9 and 10 to clarify that which Applicant considers to be the invention. Further, Applicant has amended the specification for purposes of clarification. Applicant respectfully submits that the amendments to the claims are fully supported by the originally-filed specification and that the amendments to the specification do not add new subject matter.

The rejection of claims 2-4, 8-10, 20 and 22 under 35 U.S.C. 112, second paragraph, have been addressed by amendments contained herein in accordance with the guidelines as set forth in the Office Action. Accordingly, Applicant respectfully requests that this rejection be reconsidered and withdrawn.

The rejection of claims 1-11 and 20-23 under 35 U.S.C. 112, first paragraph, is hereby traversed and reconsideration is respectfully requested in view of amendments made herein. Applicant has amended the specification to include a written description that is consistent with the claim language. Applicant notes that the material added to the specification is shown in Figure 3 of the originally-filed application in which on either side of the gate electrode 52 in both the NMOS transistor or the PMOS transistor, the lateral dimensions of the heavily doped drain and source diffusion layers 65, 66 that are disposed at a surface of the substrate are

approximately equal to and aligned with the lateral dimensions sidewall offsets 54. Accordingly, Applicant respectfully requests that this rejection be reconsidered and withdrawn.

The rejection of claims 1-4, 6, 8-10, 21 and 23 under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,545,575 to Cheng et al. (hereinafter "Cheng") is hereby traversed and reconsideration is respectfully requested.

Independent claim 1 recites a semiconductor device including a semiconductor substrate, an insulating film formed at a surface of the semiconductor substrate for defining device regions in each of which a semiconductor device is to be fabricated, and a gate electrode formed on the semiconductor substrate, the gate electrode and the insulating film defining at least one lightly doped first drain and source diffusion layer. At least one sidewall covers the gate electrode. At least one heavily doped second drain and source diffusion layer is formed at a surface of the substrate and contacted by the lightly doped first drain and source diffusion layer on at least a bottom and a lateral side. The sidewall has a sidewall offset connected thereto and extending by more than the thickness of the sidewall. The lightly doped first drain and source diffusion layer extends towards the gate electrode beyond an edge of the sidewall offset, and the heavily doped second drain and source diffusion layer extends below said sidewall offset but is spaced outwardly away from an edge of the gate electrode in a direction along said surface of said semiconductor substrate. Further, all of the at least one heavily doped second drain and source diffusion layer that is disposed at said surface of said semiconductor substrate has a lateral dimension along the surface of said semiconductor substrate that is approximately equal to and

aligned with the lateral dimension of said sidewall offset. Claims 3-5, 20 and 21 depend directly or indirectly on independent claim 1.

Independent claim 6 recites a semiconductor device including a semiconductor substrate, an insulating film formed at a surface of the semiconductor substrate for defining device regions in each of which a semiconductor device is to be fabricated, and a gate electrode formed on the semiconductor substrate, the gate electrode and the insulating film defining at least one lightly doped first drain and source diffusion layer. There is at least one sidewall covering the gate electrode, and at least one heavily doped second drain and source diffusion layer formed at a surface of the semiconductor substrate around the gate electrode, wherein the first drain and source diffusion layer contacts the second drain and source diffusion layer on at least a bottom and a lateral side. The sidewall has a sidewall offset connected thereto and extending outwardly of the gate electrode along the surface of the semiconductor substrate in at least one region below which the at least one second drain and source diffusion layer is formed. The sidewall offset extends along a lateral surface of the gate oxide film on which the gate electrode is formed by an amount that is greater than the thickness of the sidewall. Low-resistive wiring layers are formed at the surface of the drain and source diffusion layers and located outwardly beyond a peripheral edge of the sidewall and offset in at least one drain and source diffusion layer. The lightly doped first drain and source diffusion layer extends towards the gate electrode beyond an edge of the sidewall offset, and the heavily doped second drain and source diffusion layer extends below said sidewall offset but are spaced outwardly away from an edge of the gate electrode in a direction along said horizontal surface of said semiconductor substrate. Further, all of said at least one second drain and source diffusion layer that is disposed at said surface of said

semiconductor substrate has a lateral dimension along the surface of said semiconductor substrate that is approximately equal to and aligned with the lateral dimension of said sidewall offset. Claims 7, 9-11, 22 and 23 depend directly or indirectly on independent claim 6.

The Cheng reference discloses an insulated gate semiconductor device having gate electrodes, and a source region 57 nested inside source region 43, etc. Openings in a layer of dielectric material 63 expose portions of the source/drain diffusion regions to form silicide 64. (See Abstract; col. 5, lines 39-67; and Figures 7 and 15 of Cheng).

Applicant's independent claims recite a semiconductor device having at least the feature of at least one lightly doped first drain and source diffusion layer extending towards said gate electrode beyond an edge of said sidewall offset, and at least one heavily doped second drain and source diffusion layer extending below said sidewall offset but spaced outwardly away from an edge of the gate electrode in a direction along said horizontal surface of said semiconductor substrate, and *wherein all of said at least one heavily doped second drain and source diffusion layer that is disposed at said surface of said semiconductor substrate has a lateral dimension along the surface of said semiconductor substrate that is approximately equal to and aligned with the lateral dimension of said sidewall offset.* The sidewall offset prevents the second diffusion layer from being exposed at a surface of the semiconductor substrate and, accordingly, it is possible to prevent the low-resistive wiring layer from abnormally growing above the second diffusion layer. In addition, since the sidewall offset is formed only above the second drain and source diffusion layer, unnecessary increase of a chip area is prevented. This structure of the present claimed invention makes it possible for the source and drain diffusion layers, by being

outwardly spaced away from the edge of the gate electrode of a transistor, to have a high breakdown voltage and thereby prevents generation of a leakage current between bands. For purposes of example only, Applicants refer to Figure 3 of the present specification in which is shown gate electrode element 52 having a sidewall 53 and sidewall offset 54, and in which heavily doped source and drain diffusion layers 65 and 66 include portions disposed at the substrate surface and have lateral dimensions that are approximately equal to and aligned with a lateral dimension of a sidewall offset 54 extending in a direction along the substrate surface.

Applicant respectfully submits that Cheng does not teach or fairly suggest at least the above-noted features as claimed by Applicant. The Office Action cites Figures 7 and 15 of Cheng. In Figure 15, the Office Action identifies lightly doped source and drain regions, 77' and 78', heavily doped source and drain diffusion layers 82' and 84' and sidewall 66. However, it is readily apparent from this figure that the sidewall 66 extends further along the substrate surface than the portions of layers 82' and 84' disposed at the substrate surface. The lateral dimension of the portions of layers 82' and 84' disposed at the substrate surface are not approximately equal to and aligned with the lateral dimension of a sidewall offset extending along the substrate surface as is claimed by Applicant.

Moreover, in Figure 7 of Cheng, the dopant regions, see regions 57 and 58, extend beyond the peripheral edges of the sidewalls and the lateral portions disposed at the semiconductor substrate surface are not aligned with the sidewall offset. Cheng's dopant regions 57 and 58 extend below so as to overlap vertically with the gate electrode portions 49 and 52, but do not have approximately equal dimensions or nor are aligned with a lateral dimension of a

sidewall offset. Applicant respectfully submits that Cheng does not teach or fairly suggest at least the above-noted features as claimed by Applicant. Accordingly, Applicant respectfully requests that this rejection be reconsidered and withdrawn.

The rejection of claims 5, 7, 11, 21 and 23 under 35 U.S.C. 103(a) as being unpatentable over Cheng in view of U.S. Patent No. 5,316,977 to Kunishima et al. (hereinafter "Kunishima") is hereby traversed and reconsideration is respectfully requested.

The features of independent claims 1 and 6 are discussed above with respect to the Cheng reference. Claims 5, 7, 11, 21 and 23 depend therefrom.

Kunishima discloses a method of manufacturing a semiconductor device comprising metal silicide. The Kunishima reference is cited by the Office Action as disclosing a silicide layer comprising titanium silicide, using a semiconductor device as a CMOS device, and a sidewall entirely covering the gate electrode.

Applicant respectfully submits that Kunishima fails to overcome the above-noted deficiencies of the Cheng reference with respect to Applicant's claimed invention. Kunishima does not disclose the configuration and dimensions of a sidewall offset and heavily doped source and drain diffusion layers as described above with respect to Applicant's claims. As seen in Figure 3B of Kunishima, Kunishima discloses only a shallow diffusion layer 17, does not disclose a sidewall offset, and consequently, does not disclose a portion of a heavily doped second source and drain diffusion layer disposed at surface of a semiconductor substrate having a

lateral dimension that is approximately equal to and aligned with the lateral dimension of a sidewall offset. Accordingly, Applicant respectfully submits that neither Kunishima nor Cheng, taken alone or in any combination, teach or fairly the above noted features as claimed by Applicant. In view of the above, Applicant respectfully requests that this rejection be reconsidered and withdrawn.

The rejection of claims 20 and 22 under 35 U.S.C. 103(a) as being unpatentable over Cheng in view of U.S. Patent No. 5,439,835 to Gonzalez (hereinafter "Gonzalez") is hereby traversed and reconsideration is respectfully requested.

The features of independent claims 1 and 6 are discussed above with respect to the Cheng reference. Claims 20 and 22 depend therefrom.

Applicant respectfully submits that Gonzalez does not overcome the above-noted deficiencies of Cheng with respect to the Applicant's presently claimed invention. Gonzalez discloses a gate electrode, sidewall and sidewall offset and drain and source regions (see, for example, Figures 7-9 of Gonzalez), but the sidewall of Gonzalez below which are positioned multiple drain and source regions does not include a sidewall offset. Further, as seen for example in Figures 8 and 9, Gonzalez's N-implant region 81 has a portion under a sidewall; however the region disposed at the semiconductor substrate surface further extends laterally along the substrate surface *beyond the sidewall*. Consequently, Gonzalez contains no disclosure of a sidewall offset that is aligned with a heavily doped drain and source diffusion layer and wherein all of said at least one heavily doped second drain and source diffusion layer that is

disposed at said surface of said semiconductor substrate has a lateral dimension along the surface of said semiconductor substrate that is approximately equal to and aligned with the lateral dimension of said sidewall offset. Accordingly, Applicant respectfully submits that neither Gonzalez nor Cheng, taken alone or in any combination, teach or suggest at least the above features as claimed by Applicant. In view of the above, Applicant respectfully requests that this rejection be reconsidered and withdrawn.

Based on the above, Applicants respectfully request that the Examiner reconsider and withdraw all outstanding rejections and objections. Favorable consideration and allowance are earnestly solicited. Should there be any questions after reviewing this paper, the Examiner is invited to contact the undersigned at 617-248-4038.

Respectfully submitted,
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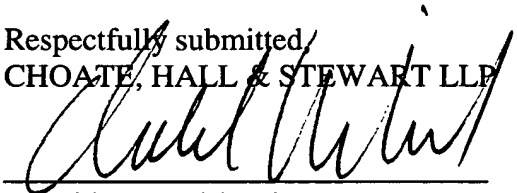

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